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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/623,397	07/18/2003	Peyman Hadizad	ONS00501	4648

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EXAMINER	
SOWARD, IDA M	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 03/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/623,397	HADIZAD, PEYMAN	
	Examiner	Art Unit	
	Ida M Soward	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 July 2003*.

2a)☐ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *10-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,7 and 8* is/are rejected.

7)☒ Claim(s) *5,6 and 9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 July 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☒ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7-18-03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

This application contains claims directed to the following patentably distinct species of the claimed invention: claims 1-9 (Vertical FET Device), claims 10-16 (Semiconductor Switching Device) and claims 17-20 (Compound Semiconductor Vertical FET Device).

Applicant is required under 35 U.S.C. 121 to elect a single disclosed species for prosecution on the merits to which the claims shall be restricted if no generic claim is finally held to be allowable.

Applicant is advised that a reply to this requirement must include an identification of the species that is elected consonant with this requirement, and a listing of all claims readable thereon, including any claims subsequently added. An argument that a claim is allowable or that all claims are generic is considered nonresponsive unless accompanied by an election.

Upon the allowance of a generic claim, applicant will be entitled to consideration of claims to additional species which are written in dependent form or otherwise include all the limitations of an allowed generic claim as provided by 37 CFR 1.141. If claims are added after the election, applicant must indicate which are readable upon the elected species. MPEP § 809.02(a).

Should applicant traverse on the ground that the species are not patentably distinct, applicant should submit evidence or identify such evidence now of record

showing the species to be obvious variants or clearly admit on the record that this is the case. In either instance, if the examiner finds one of the inventions unpatentable over the prior art, the evidence or admission may be used in a rejection under 35 U.S.C. 103(a) of the other invention.

During a telephone conversation with James J. Stipanuk on 2-25-04 a provisional election was made without traverse to prosecute the invention of a vertical FET device, claims 1-9. Affirmation of this election must be made by applicant in replying to this Office Action. Claims 10-20 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Priority

If applicant desires priority under 35 U.S.C. 119(e) or 120 based upon a previously filed application, specific reference to the earlier filed application must be made in the instant application. For benefit claims under 35 U.S.C. 120, 121 or 365(c), the reference must include the relationship (i.e., continuation, divisional, or continuation-in-part) of the applications. This should appear as the first sentence of the specification following the title, preferably as a separate paragraph unless it appears in an application data sheet. The status of nonprovisional parent application(s) (whether patented or abandoned) should also be included. If a parent application has become a patent, the expression "now Patent No. _____" should follow the filing date of the parent application. If a parent application has become abandoned, the expression "now abandoned" should follow the filing date of the parent application.

If the application is a utility or plant application filed under 35 U.S.C. 111(a) on or after November 29, 2000, the specific reference must be submitted during the pendency of the application and within the later of four months from the actual filing date of the application or sixteen months from the filing date of the prior application. If the application is a utility or plant application which entered the national stage from an international application filed on or after November 29, 2000, after compliance with 35 U.S.C. 371, the specific reference must be submitted during the pendency of the application and within the later of four months from the date on which the national stage commenced under 35 U.S.C. 371(b) or (f) or sixteen months from the filing date of the prior application. See 37 CFR 1.78(a)(2)(ii) and (a)(5)(ii). This time period is not extendable and a failure to submit the reference required by 35 U.S.C. 119(e) and/or 120, where applicable, within this time period is considered a waiver of any benefit of such prior application(s) under 35 U.S.C. 119(e), 120, 121 and 365(c). A priority claim filed after the required time period may be accepted if it is accompanied by a grantable petition to accept an unintentionally delayed claim for priority under 35 U.S.C. 119(e), 120, 121 and 365(c). The petition must be accompanied by (1) the reference required by 35 U.S.C. 120 or 119(e) and 37 CFR 1.78(a)(2) or (a)(5) to the prior application (unless previously submitted), (2) a surcharge under 37 CFR 1.17(t), and (3) a statement that the entire delay between the date the claim was due under 37 CFR 1.78(a)(2) or (a)(5) and the date the claim was filed was unintentional. The Director may require additional information where there is a question whether the delay was

unintentional. The petition should be addressed to: Mail Stop Petition, Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Drawings

The informal drawings are not of sufficient quality to permit examination. Accordingly, new drawings are required in reply to this Office action.

Applicant is given a TWO MONTH time period to submit new drawings in compliance with 37 CFR 1.81. Extensions of time may be obtained under the provisions of 37 CFR 1.136(a). Failure to timely submit new drawings will result in **ABANDONMENT** of the application.

Claim Rejections - 35 USC § 103

Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kocon et al. (US 6,673,681 B2) in view of Fujishima et al. (US 2002/0112363 A1).

Kocon et al. teach vertical FET device comprising: body of semiconductor material comprising a first conductivity type, wherein the body 201 of semiconductor material having an upper surface and a lower surface opposing the upper surface, wherein the lower surface provides a drain contact 219; a first trench 203 formed in the body of semiconductor material and extending from the upper surface, wherein the first trench has a first width, a first depth from the upper surface, first sidewalls, and a first bottom surface; second trench 204 formed within the first trench, wherein the second trench has a second width, a second depth from the first surface, second; sidewalls and

a second bottom surface, wherein the first and second trenches form a first trench structure; first source region 214 formed in the body semiconductor material extending from the upper surface; and a first doped gate region 207 of a second conductivity type (Figure 2, cols. 3-4, lines 34-67 and 2-23, respectively).

However, Kocon et al. fail to teach a first source region spaced apart from the first trench; and a gate region formed in at least a portion of the second sidewalls and the second bottom surface. Fujishima et al. teach a first source region 202 spaced apart from the first trench; and a gate region 210 formed in at least a portion of the second sidewalls and the second bottom surface (Figure 27a, page 5, paragraph [0086]). Since Kocon et al. and Fujishima et al. are from the same field of endeavor (vertical FET devices), the purpose disclosed by Fujishima et al. would have been pertinent in the art of Kocon et al. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the vertical FET device as taught by Kocon et al. with the vertical FET device having a gate and spaced apart source region as taught by Fujishima et al. to provide a structure with a high breakdown voltage and low on-resistance (page 1, paragraph [0002]).

Claims 2-3 and 7-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kocon et al. (US 6,673,681 B2) and Fujishima et al. (US 2002/0112363 A1) as applied to claim 1 above, and further in view of Chatterjee et al. (5,208,657).

Kocon et al. and Fujishima et al. teach all mentioned in the rejection above. However, Kocon et al. and Fujishima et al. Fail to teach a body of semiconductor

material comprising a III-V semiconductor substrate having a first dopant concentration and a first epitaxial layer formed on a surface of the semiconductor substrate, wherein the first epitaxial layer has a second dopant concentration less than the first dopant concentration; a body of semiconductor material comprising one of GaAs or InP; and a depletion mode FET device.

In regard to claim 2, Chatterjee et al. teach a body of semiconductor material comprising a III-V (col. 13, lines 55-60) semiconductor substrate 332 having a first dopant concentration P+ and a first epitaxial layer 344 formed on a surface of the semiconductor substrate, wherein the first epitaxial layer has a second dopant concentration P less than the first dopant concentration P+ (Figure 10, col. 10, lines 15-56).

In regard to claim 3, Chatterjee et al. teach a body of semiconductor material comprising one of GaAs or InP (col. 13, lines 55-60).

In regard to claims 7-8, Chatterjee et al. teach a depletion mode FET device (cols. 5 and 13, lines 13-22 and 63-68, respectively).

Since Kocon et al., Fujishima et al. and Niu et al. are from the same field of endeavor (semiconductor structures), the purpose disclosed by Niu et al. would have been pertinent in the art of Kocon et al. and Fujishima et al. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the vertical FET device as taught by Kocon et al. and the vertical FET device having a gate and spaced apart source region as taught by Fujishima et al. with the vertical FET device having GaAs or InP semiconductor material as taught by Chatterjee

et al. to provide a modification that does not disrupt the off/on function of the transistor (col. 13, lines 24-29).

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kocon et al. (US 6,673,681 B2) and Fujishima et al. (US 2002/0112363 A1) as applied to claim 1 above, and further in view of Niu et al. (US 6,277,751 B1).

Kocon et al. and Fujishima et al. teach all mentioned in the rejection above. However, Kocon et al. and Fujishima et al. fail to teach a first passivation layer formed over the doped gate region; and a planarized passivation layer formed over the first passivation layer. Niu et al. teach a first passivation layer 202 formed over structures; and a planarized passivation layer 204 formed over the first passivation layer (Figure 2B, col. 3, lines 28-67). Since Kocon et al., Fujishima et al. and Niu et al. are from the same field of endeavor (semiconductor structures), the purpose disclosed by Niu et al. would have been pertinent in the art of Kocon et al. and Fujishima et al. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the vertical FET device as taught by Kocon et al. and the vertical FET device having a gate and spaced apart source region as taught by Fujishima et al. with the passivation layers of Niu et al. to provide a planarization method to prevent the formation of recess cavity above an insulating layer (col. 2, lines 26-31).

Allowable Subject Matter

Claims 5-6 and 9 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following patents are cite to further show the state of the are with respect to vertical FET devices:

Lechaton et al. (4,661,832) Lee (US 20020058381 A1)

Malhi (4,651,184) Malhi (5,326,711).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ida M Soward whose telephone number is 571-272-1845. The examiner can normally be reached on Monday - Thursday, 6:30 am to 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

IMS
March 5, 2004

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